

The IET9121/23 is a small form factor Intelligent Ethernet Module (IEM) that integrates a high performance (100 MIPS) 8051 microcontroller with 128Kbyte FLASH, 8448 Bytes of RAM, a 10/12 bit ADC, an 8 bit high speed ADC, 2 UARTS, SMBus™, I<sup>2</sup>C™, SPI™ and a 5 channel programmable counter array. The module also features a high performance ethernet controller making this module an excellent choice for embedded applications needing ethernet connectivity.

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The IET9121/23 IEM is built around two highly integrated devices, the Silabs C8051F121/123 MCU and the Davicom DM9000E ethernet controller. Both devices represent the latest technology in their field and were selected to give the user maximum performance with the right cost.

The module is 100% pin for pin compatible with the IET9021/23 modules.

#### C8051F121/123 MCU

This device holds the powerful CIP-51 MCU core, which is capable of peaking an astonishing 100MIPS. It also entails a large number of on chip peripherals as well as 128Kbytes of in application programmable FLASH memory and 8Kbyte XRAM + 256Byte IRAM. This allows the module to adapt to numerous applications. The IET9121/23 can map the following of the on-chip peripherals to its pins:

- 4 single or 2 differential 10/12-bit ADC0 channels with programmable gain amplifier.
- Up to 7 channels 8-bit 500 ksps ADC with programmable gain amplifier.
- 2 analog comparator channels
- 2 12 bit DAC's
- UART 2 channels
- SMBus (I2C Bus compatible)
- SPI bus
- 5 capture/compare modules
- 5 general purpose timer/counters

The on chip peripherals are connected to the module pins via the internal MCU crossbar.

The module is available in two different versions with different ADC0 resolution. The IET9121 contains the MCU C8051F121 where the ADC0 resolution is 12-bits and IET9123 contains the C8051F123 MCU where the ADC0 resolution is 10-bits.



#### DM9000E Ethernet Controller

The DM9000E is a 10/100 Mbit/s Ethernet controller designed for embedded applications. As such it interfaces directly without any glue logic to the MCU. All discrete ethernet filter components are placed on the board and the application board only needs to supply the transformers and connector. We recommend the use of a connector with the transformers integrated. The evaluation base module uses the J00-0045 device from Pulse Engineering, which works very good.

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#### Technical Data:

Measures (mm): 54 x 34.5  
 Connector 1: 2 row headers (40-pins)  
 Microcontroller: C8051F121/123  
 Ethernet Chip: Davicom DM9000E

#### Ordering Information:

IET9121E, Bulk packed board with C8051F121  
 IET9123E, Bulk packed board with C8051F123  
 IET9121E-DK1, Development kit with IET9121  
 IET9123E-DK1, Development kit with IET9123

#### RoHS, WEEE compliance

All products comply with the European RoHS and WEEE directives

**General Information**

The module was designed to give the user an easy and cost effective way to implement LAN and Internet connectivity with minimal effort. The Silabs MCU was selected due to its ability to be dynamically configured, allowing the user to adapt the module to fit his/her needs and its very high execution speed.

The modules flexible design including high resolution ADC's makes it possible to use it in a variety of applications and environments.

An on board low-dropout voltage regulator makes it possible to source the board from a 4-7 volt power source eliminating the need for a 3.3Volt voltage regulator on the application board.

There is only one crystal on board, which is driving the ethernet controller. The MCU therefore operates from the internal calibrated 24.5MHz clock divided by 8 (3,0625MHz) after reset. The CK20 (a fixed 20 MHz clock signal) output of the DM9000E is connected to the XTAL1 input of the MCU and can be selected as the master clock by the MCU giving you a master clock of 20MHz instead.

An internal PLL in the microcontroller can be used to boost the performance of the controller by dividing and multiplying the clock source.

The PCB is a 4-layer design with separate ground planes for all power sections giving the module excellent analog performance and a minimum of emitted noise.

**Module Pin Out**

POWER	1	40	TXO-
ACTIVITY	2	39	TXO+
FULL_DUP	3	38	EGND
SPEED100	4	37	RXI-
GPIO2	5	36	RXI+
GPIO1	6	35	3.3V
P0.5	7	34	P1.0
P0.4	8	33	P1.1
P0.3	9	32	P1.2
P0.2	10	31	P1.3
P0.1	11	30	P1.4
P0.0	12	29	P1.5
DGND	13	28	P1.6
AGND	14	27	DGND
DAC1	15	26	AIN0.3
DAC0	16	25	AIN0.2
CP0+	17	24	AIN0.1
CP0-	18	23	AIN0.0
CP1+	19	22	VREFA
CP1-	20	21	VREF

Pin Description:

- VREF (I) – Reference voltage pin.  
 Reference voltage input for the on board analog circuitry.
- VREFA (O) – Reference voltage output  
 Reference voltage output from the module.  
 Can be tied to VREF input.
- AGND (P) – Analog Ground  
 This pin is connected to the analog ground plane on the module.
- AIN0.X (I) – 10/12 bit ADC0 input.  
 Inputs to the 10/12 bit AD converter.
- DGND (P) – Digital Ground  
 Digital ground.
- P1.X (I/O) – Port 1 signals  
 General I/O pins which can be mapped to the appropriate peripheral function.
- VCC (P) – 3.3 Volt input or output  
 When the on board voltage regulator is enabled this pin can source 3.3V/50mA.  
 Otherwise you have to source this power pin with 3.3V/80mA.
- GPIOX (I/O) – General purpose digital I/O pins.  
 Connected to the DM9000E general-purpose I/O pins.
- SPEED\_100 (O) – LED driver pin  
 100Mbit indicator LED output. Connect to the cathode of a LED.
- FULL\_DUP (O) – LED driver pin  
 Full duplex indicator LED output. Connect to the cathode of a LED.
- ACTIVITY (O) – LED driver pin  
 LAN activity LED output. Connect to the cathode of a LED.
- CP0+ (I) – Comparator positive input  
 Input connected to the positive side of the comparator.
- CP0- (I) – Comparator negative input  
 Input connected to the negative side of the comparator.
- DACX (O) – DAC output.  
 Digital to Analog output.  
 Signals used for downloading code and/or debugging the system during development.

**P1.X (I/O) – Port 1 signals**

General I/O pins or mapped to the corresponding peripheral function.

**POWER (P) – Voltage Input**

4-15 Volt power input. Only if the on-board regulator is enabled.

**RXI+ / RXI- (I) – Ethernet Input signals**

Ethernet Receiver input signals. Connect directly to the ethernet input transformer.

**EGND (P) – Ethernet Analog Ground**

Ground Plane for the Ethernet signals. Must be used to shield the Ethernet signals on the application board and to ground the filtering capacitors on the Ethernet transformer.

**TXO+ / TXO- (O) Ethernet Output signals**

Ethernet transmitter output signals. Connect directly to the ethernet output transformer.

**Module Memory**

On board you will find 128Kbytes of FLASH memory for program storage, 8Kbytes of SRAM in XMEM space for data storage and 256 bytes of IRAM for variable and data storage.

**FLASH**

The MCU include 128KBytes on-chip, re-programmable FLASH memory for program code or non-volatile data storage. An additional 256-byte page of FLASH is also included for non-volatile data storage. The FLASH memory can be programmed in system through the JTAG interface, or by software using the MOVX write instructions. Once cleared to logic 0, a FLASH bit must be erased to set it back to logic 1. Bytes should be erased (set to 0xFF) before being reprogrammed. FLASH write and erase operations are automatically timed by hardware for proper execution. During a FLASH erase or write, the FLBUSY bit in the FLSTAT register is set to '1'. During this time, instructions that are located in the prefetch buffer or the branch target cache can be executed, but the processor will stall until the erase or write is completed if instruction data must be fetched from FLASH memory. Interrupts that have been pre-loaded into the branch target cache can also be serviced at this time, if the current code is also executing from the prefetch engine or cache memory. Any interrupts that are not pre-loaded into cache, or that occur while the core is halted, will be held in a pending state during the FLASH write/erase operation, and serviced in priority order once the FLASH operation has completed.

**XRAM**

The Silabs MCU can access two types of XMEM data. The first is the on-chip XRAM that is located on-chip of the MCU. This memory occupies XMEM memory area from 0x0000 – 0x1FFF.

The second type of data is of-chip XMEM data.

The only of-chip unit found on this module is the ethernet controller, discussed in the next section. While reading or writing data from/to the external memory bus, signals RD, WR and ALE are activated and a read or write cycle takes place.

**MCU <-> Ethernet Controller Interface**

The ethernet controller is connected to the MCU through the external memory interface.

This effectively means that the DM9000E will be mapped into the entire free XMEM memory space from 0x2000 – 0xFFFF.

We recommend that you use the following addresses when accessing the DM9000E in order to keep your software compatible with future products.

DM9000E Data Register	0x8100
DM9000E Register Select	0x8000

**Microcontroller Crossbar**

The most compelling feature of the C8051F121/123 MCU is its ability to dynamically configure the use of its internal peripherals.

The crossbar allocates and assigns port pins on Port 0 and Port 1 to the on-chip digital peripherals using a priority order. The port pins are allocated in order starting with port pin P0.0 (Port 0 pin 0) and continue through P1.6 (Port 1 pin 6) if necessary. The digital peripherals are assigned port pins in a priority order with UART0 having the highest priority and CNVSTR having the lowest priority.

For a close description and examples on how to configure the crossbar please read the Silabs documentation.

**UARTs**

UART0 and UART1 are two enhanced serial ports with frame error detection and address recognition hardware. The UARTs may operate in full-duplex asynchronous or half-duplex synchronous modes, and multiprocessor communication is fully supported. Receive data is buffered in a holding register, allowing the UARTs to start reception of a second incoming data byte before software has finished reading the previous data byte. A Receive Overrun bit indicates when new received data is latched into the receive buffer before the previous

received byte is read.

The UARTs are accessed via their associated SFRs, Serial Control (SCONx) and Serial Data Buffer (SBUFx). The single SBUFx location provides access to both transmit and receive registers. Reads access the Receive register and writes access the Transmit register automatically.

The UARTs may be operated in polled or interrupt mode. Two sources of interrupts are available: a Transmit Interrupt flag, TI0 (SCONx.1) set when transmission of a data byte is complete, and a Receive Interrupt flag, RI0 (SCONx.0) set when reception of a data byte is complete. UART interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine; they must be cleared manually by software. This allows software to determine the cause of the UART interrupt (transmit complete or receive complete).

### I2C/SMBus

The SMBus0 I/O interface is a two-wire, bi-directional serial bus. SMBus0 is compliant with the System Management Bus Specification, version 1.1, and compatible with the I2C serial bus.

Reads and writes to the interface by the system controller are byte oriented with the SMBus0 interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the system clock if desired (this can be faster than allowed by the SMBus specification, depending on the system clock used).

A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus. SMBus0 may operate as a master and/or slave, and may function on a bus with multiple masters. SMBus0 provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation.

### SPI

The Serial Peripheral Interface (SPI0) provides access to a four-wire, full-duplex, serial bus. SPI0 may operate as a master or a slave, and supports the connection of multiple slaves and masters on the same bus. A slave-select input (NSS) is included in the SPI0 interface to select SPI0 as a slave; additional general purpose port I/O can be used as slave-select outputs when SPI0 is operating as a master. Collision detection is provided when two or more masters attempt a data transfer at the same time.

When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency. When the SPI is configured

as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency.

In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

### Timer Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. PCA0 consists of a dedicated 16-bit counter/timer and five 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled.

The counter/timer is driven by a programmable timebase that can select between six inputs as its source: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflow, or an external clock signal on the ECI line.

Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM. The PCA is configured and controlled through the system controller's Special Function Registers.

### Analog Inputs (ADC0)

The ADC0 subsystem for the MCU consists of a 9-channel, configurable analog multiplexer (AMUX0) of which 4 channels is routed to the IET9121/23 module connectors. Connected to this is a programmable gain amplifier (PGA0), and a 100 kps, 10/12-bit successive-approximation-register ADC with integrated track-and-hold and Programmable Window Detector.

The AMUX0, PGA0, Data Conversion Modes, and Window Detector are all configurable under software control via Special Function Registers. The ADC0 subsystem (ADC0, track-and-hold and PGA0) is enabled only when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1. The ADC0 subsystem is in low power shutdown when this bit is logic 0.

### Analog Inputs (ADC2)

The ADC1 subsystem for the C8051F121/123 consists of an 8-channel, configurable analog multiplexer (AMUX2), with 7 channels routed to the pins of the module. A programmable gain amplifier (PGA2), and a 500 ksp/s, 8-bit successive-approximation register ADC with integrated track-and-hold. The AMUX2, PGA2, and Data Conversion Modes, are all configurable under software control via the Special Function Registers.

The ADC2 subsystem is enabled only when the AD2EN bit in the ADC2 Control register (ADC2CN) is set to logic 1. The ADC2 subsystem is in low power shutdown when this bit is logic 0.

### Analog Outputs

Each IET9121/23 device includes two on-chip 12-bit voltage-mode Digital-to-Analog Converters (DACs). Each DAC has an output swing of 0V to (VREF-1LSB) for a corresponding input code range of 0x000 to 0xFFFF. The DACs may be enabled/disabled via their corresponding control registers, DAC0CN and DAC1CN. While disabled, the DAC output is maintained in a high-impedance state, and the DAC supply current falls to 1  $\mu$ A or less.

The voltage reference for each DAC is supplied at the VREF pin. Note that the VREF pin may be driven by the internal voltage reference pin VREFA or an external source. If the internal voltage reference is used it must be enabled in order for the DAC outputs to be valid.

### Development Support

In order to start developing your own applications for the IET9121/23 you need to have a C-compiler/Assembler/Linker, a debugger and a target hardware. We provide support for a number of different development systems.

### Silabs Environment

This environment is the most comprehensive that will allow full speed non-intrusive debugging of the module via the JTAG interface. When purchasing one of our development kits (DK1/DK2) you receive a JTAG programming adapter that is used for both

downloading code and debugging the system. On the CD ROM we have also included the free SDCC compiler which integrates seamlessly into the Silabs IDE. The SDCC compiler can easily be replaced with a Keil compiler giving you the maximum performance.

Please note that we do not provide the Keil C-compiler. This has to be purchased separately.

### uC/51 Tool-chain

The uC/51 tool-chain provides you with a highly optimizing C-compiler. As of revision 1.2.04 this toolchain also supports in circuit debug through the Silabs IDE.

### Documentation List

This is a list of relevant documentation that you will need to refer to when writing programs for the IET9121/23 module.

- C8051F121/123 Data Sheet
- DM9000E Data Sheet
- DM9000E Application Note

### Technical Data:

Parameter	Min	Typ	Max
POWER* (V)	3.7	-	7
VCC (V)	3.135	3.3	3.465
Power Dissipation (mA)	-	-	165
MCU Frequency (MHz)	-	-	100

**Revision History (Latest rev. first)**

<b>Rev</b>	<b>Date</b>	<b>Comment</b>
PA1		First layout
B	07-03-05	Minor updates to the layout. Added conformance statements.

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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

NOTES: